Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of the Claims:

Claim 1. (Canceled)

2. (Previously Presented) The integrated circuit claim of 11, wherein the means for receiving test results comprises a test response analysis unit for compressing test response vectors, the integrated circuit further comprising a test control block for controlling the test procedure.

3. (Canceled)

4. (Previously Presented) The tester of claim 10, comprising a test response analysis unit arranged to compress test response vectors received from the integrated circuit to be tested.

5. (Previously Presented) The tester of claim 10, wherein the programmable test vector generator is a programmable algorithmic test vector generator which includes an arithmetic and logic unit and generates test vectors in real time.

6. (Canceled)

7. (Canceled)

8. (Canceled)

9. (Canceled)

10. (Previously Presented) A tester for testing logic circuitry of an integrated circuit, comprising a programmable test vector generator for generating test vectors for the logic circuitry.

11. (Previously Presented) An integrated circuit comprising:

means for receiving from an external tester test vectors for testing logic circuitry; and

means for receiving from the logic circuitry test results in response to the test vectors, for producing a compact representation of said test results; and for outputting said compact representation to the external tester.

12. (Previously Presented) A method of testing logic circuitry of an integrated circuit, comprising:

generating within an external tester test vectors for the logic circuitry, using a programmable test vector generator; and

the integrated circuit receiving the test vectors and applying the test vectors to the logic circuitry.

13. (Previously Presented) The method of claim 12, wherein the integrated circuit includes a test response analysis unit, further comprising:

receiving from the logic circuitry test results in response to the test vectors;

producing a compact representation of said test results; and

outputting said compact representation to the external tester.

14. (New) The method of claim 13 wherein said compact representation includes test vectors applied directly to the external tester to enable fault localization on the logic circuitry.

CONCLUSION

In view of the above arguments and amendments provided in the Response to Office Action mailed July 28, 2005, Applicant believes that all pending claims are allowable and respectfully request a Notice of Allowance for this application from the Examiner.

Respectfully submitted,
NORTH WEBER & BAUGH

Nov. 16, 2005

Michael V. North
Reg. No. 46,963
North Weber & Baugh LLP
2479 E. Bayshore Rd., Ste. 707
Palo Alto, CA 94303